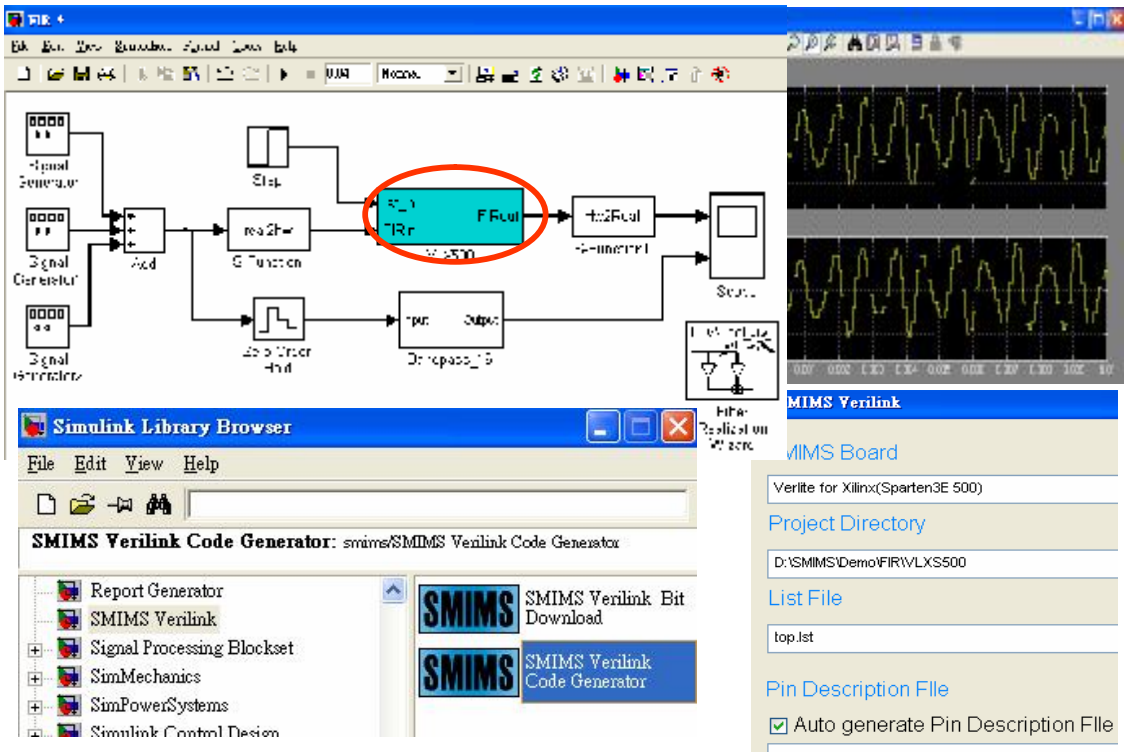
SMIMS

VeriLink®

Matlab
Simulink



Overview

Verilink® is a high-level tool connecting Matlab®/Simulink® with SMIMS® FPGA board that performs reliable verification of your distinguished design. The Verilink® for Matlab® brings the FPGA hardware platform to the heart of the acclaimed MATLAB® technical environment.

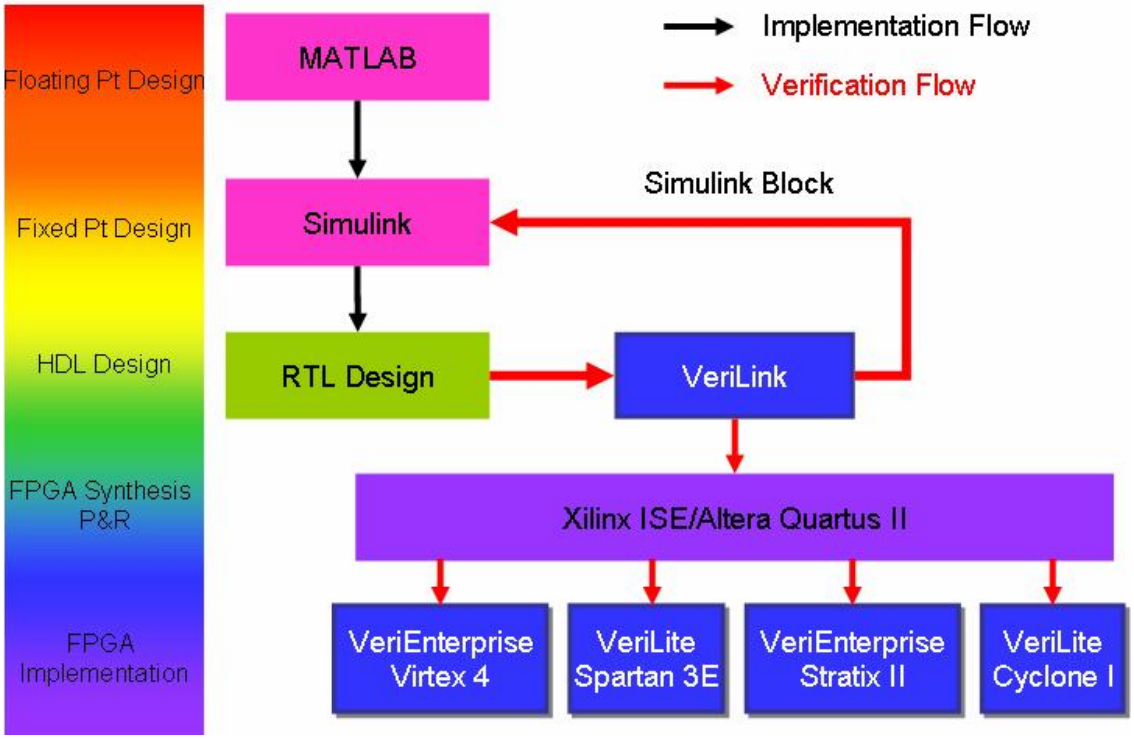
Building upon Simulink® from MathWork®, along with the VeriLink® from SMIMS®, the overall solutions allow users to quickly perform a hardware and software co-simulation for their applications.

VeriLink® shortens the design cycles by helping you to create the hardware representation of your design in the Verilink algorithm-friendly development environment. With ready HDL design, in clicks, users can automatically feed binary to SMIMS FPGA and review the result in Simulink® environment. By taking the advantages of the existing MATLAB® functions and Simulink® blocks to link with FPGA prototype, users can accomplish system-level design easily and quickly.

Key Features

- ü Link the MathWorks® MATLAB®/ Simulink® with SMIMS® FPGA Platforms
- ü HW/SW co-simulation. Accelerate system-level co-simulation with Simulink® and create an “FPGA-in-the-loop” simulation target.
- ü Export the HDL code to the Simulink® block
- ü Export the FPGA download file to the Simulink® block.
- ü Automatically produce an FPGA configuration bitstream for your HDL design
- ü Support all SMIMS® FPGA Platforms of Xilinx®/Altera®

Design Flow



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