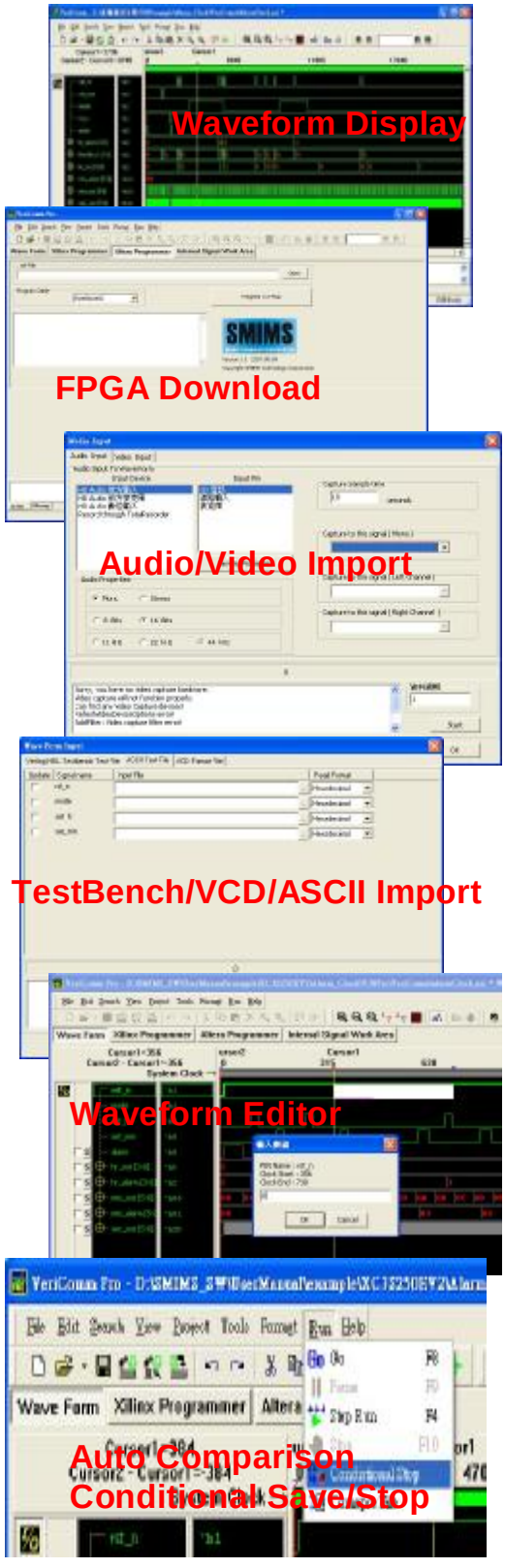
SMIMS

VeriComm® Pro



Overview

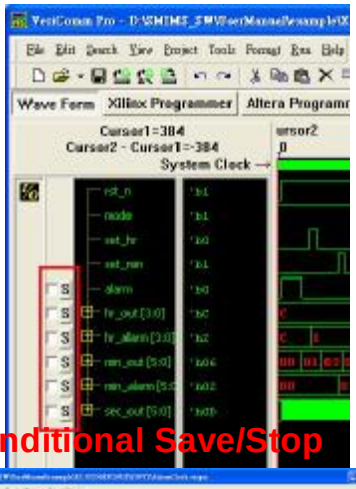
SMIMS VeriComm® Pro provides an easy-to-use verification environment which allows easy and quick debugging/analysis for a HDL-based circuit on SMIMS FPGA Platform. User-friendly GUI and multiple signal representation views make VeriComm Pro become a very powerful verification interface between the user circuit and real world signals. VeriComm Pro can import the input signals easily from PC into the user-designed circuit and export the output signals to PC for observation. With VeriComm Pro, almost all PC peripheral devices become user-designed circuit's I/Os and no real hardwired I/O device is needed for early-stage verification. The VeriComm Pro also provides the automated compilation flow, fast and easy FPGA download, and interface to SMIMS FPGA Platform for data transfer.

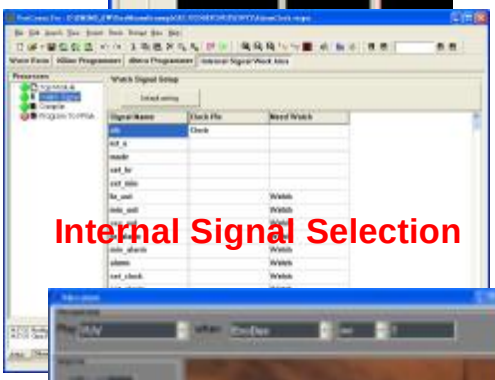
The VeriComm® Pro supports the most popular input formats which include ASCII text file, testbench, VCD, waveform editor, audio signals from microphone and video/image signals from webcam etc. The output waveform of user-designed circuit can be transformed to ASCII text format which can be compared automatically with user-specified files. Users can apply the audio/video players in VeriComm Pro to play the multimedia output signals of their circuits, and FFT to transform signals from the time domain to frequency domain.

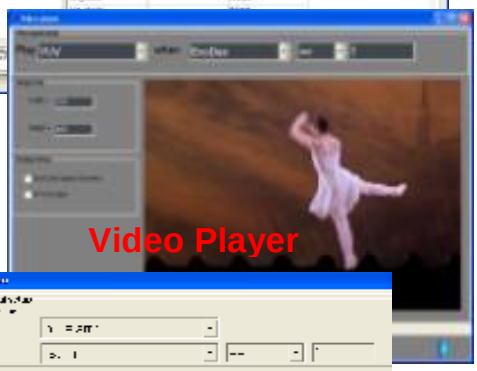
The feature of internal signal debugger in VeriComm Pro allows you to view any internal signals or nodes. A tree view GUI is offered for internal signal selection. With the help of internal signal debugger, the verification time for a user's circuit can be reduced up to 50%.

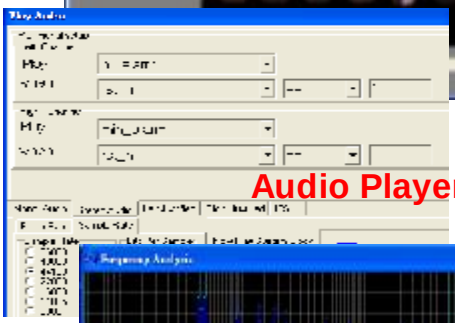
Key Features

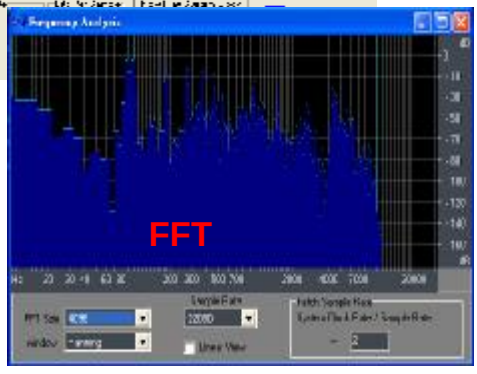
- ü Support for 32 and 64-bit Windows-based platform
- ü Input format
  - Ÿ ASCII Text import
  - Ÿ Testbench import
  - Ÿ VCD dump import
  - Ÿ Waveform editor
  - Ÿ Audio import from Microphone
  - Ÿ Video/Image import from Webcam
- ü Waveform Display
  - Ÿ Zoom in/Zoom out/Zoom all
  - Ÿ Search by edge/value
  - Ÿ Bookmark
  - Ÿ Group a bus
- ü Output waveform to ASCII Text file
- ü FPGA HDL Debugger
  - Ÿ Up to 1024 internal trace signals
  - Ÿ RTL level
  - Ÿ Internal signal selection GUI
- ü Auto Comparison with golden patterns
- ü Conditional Save/Stop
- ü Video Player
  - Ÿ YUV 420/RGB format
  - Ÿ MPEG-1/MPEG-2/MPEG-4 format
  - Ÿ Frame rare selection
  - Ÿ User-defined resolution
- ü Audio Player
  - Ÿ Parallel and most popular serial format
  - Ÿ Mono and stereo
  - Ÿ 8- and 16-bit width
- ü FFT
  - Ÿ N-point FFT
  - Ÿ Hanning, Hamming, Blackmann and Blackmann-Harris window
- ü Compile Verilog/VHDL by Xilinx ISE/Altera Quartus II
- ü Download programmer
  - Ÿ Support USB download.
  - Ÿ Fast and easy FPGA download from PC











Contact us for more information:

Taiwan
Phone: 886-2-23700590
Phone: 886-6-2381237